

**SYSTEM AND METHOD FOR VERIFYING LARGE-SCALE COMPUTING
SYSTEMS USING AN ABSTRACT VERIFICATION ENVIRONMENT**

Abstract of the Disclosure

A system and method of verifying an electronic system. A verification kernel is provided and the electronic system is expressed as a logic design. A wrapper is defined, wherein the wrapper is an interface between the logic design and the verification kernel. Tests to be run against the logic design are placed within a diagnostic program and an interface between the diagnostic program and the verification kernel is defined. The tests are then executed against the logic design. The results of the tests are captured and validated against expected results.

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. 1.10 on the date indicated below and is addressed to the Assistant Commissioner for Patents, Attn: Box Patent Application, Washington, D. C. 20231.

"Express Mail" mailing label number **EL284617661US**

Date of Deposit **October 15, 1999**

Printed name **Chris Hammond**

Signature **Chris Hammond**